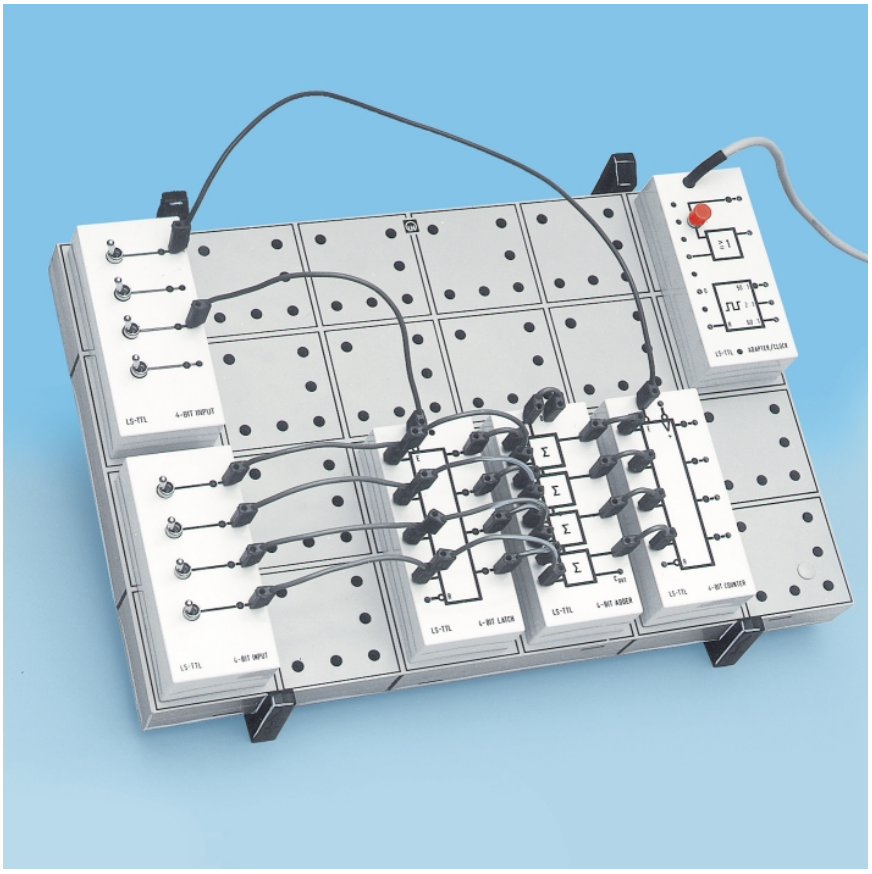

Serial and parallel adders and subtracters (P 4.4.3.3)

P 4.4.3

Serial and parallel arithmetic units

P 4.4.3.1 Data transfer between registers
P 4.4.3.2 Serial and parallel logic elements
P 4.4.3.3 Serial and parallel adders and subtracters
P 4.4.3.4 Functions of the buffer, latch and accumulator

Cat. No.	Description	P 4.4.3.1-4
571 011	SIMULOG LS-TTL, P 1 basic logic circuits	1
571 022	SIMULOG LS-TTL extension P 2 switching networks and units	1
571 044	SIMULOG LS-TTL extension E 4 serial and parallel arithmetic units	1
571 29	Base plate DIN A4 for SIMULOG LS-TTL	1
522 33	Regulated power supply, 2 x 5 V DC/1.0 A	1
571 21	Set of 5 connecting leads, 4 cm	4
571 22	Set of 5 connecting leads, 8 cm	2
571 23	Set of 5 connecting leads, 15 cm	2
571 24	Set of 5 connecting leads, 30 cm	2

In information technology, the hardware executes arithmetic, Boolean and other operations using arithmetic units. The operations can be performed either serially or in parallel.

The first three experiments investigate the serial and parallel processing of data in registers, logic elements and adders and subtracters.

The final experiment demonstrates the function of the buffer as a bus driver, the latch as a small intermediate storage element and the accumulator as a register which supports arithmetic operations.